REMARKS

Claims 1-3, 6-10, 13-17, 20-25, and 28-30, are pending in the present application. Claims 1-32 were presented for examination. Claims 4, 5, 11, 12, 18, 19, 26, 27, 31, and 32 have been cancelled by amendment.

In the office action mailed May 15, 2006 (the "Office Action"), the Examiner rejected claims 1, 15, and 28 under an obviousness-type double patenting rejection as being unpatentable over claims 1, 3, and 7 of U.S. Patent No. 6,754,117 to Jeddeloh (the "Jeddeloh I patent"). The Examiner further rejected claims 9-14 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 1 and 15 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,085,339 to Jeddeloh (the "Jeddeloh II patent"). Claims 1, 15, 23-25, and 28-30 were further rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No. 20020194558 to Wang *et al.* (the "Wang reference"). Claims 2, 6, 9, 13, 17, and 20 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Wang reference in view of U.S. Patent No. 6,732,203 to Kanapathippillai *et al.* (the "Kanapathippillai patent"). Claims 3, 10, and 16 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Wang reference in view of U.S. Patent Application Publication No. 20040216018 to Cheung (the "Cheung reference"). Claims 4, 11, and 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Wang reference in view of U.S. Patent No. 6,351,834 to Maekawa *et al.* (the "Maekawa patent"). Claims 5, 12, 19, 26, 27, 31, and 32 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Wang reference in view of U.S. Patent No. 6,487,648 to Hassoun (the "Hassoun patent"). Claims 7, 14, 21 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Wang reference in view of U.S. Patent Application Publication No. 20020199136 to Ku (the "Ku reference"). Claims 8 and 22 were rejected under 35 U.S.C. 103(a) as being unpatentable over the Wang reference in view of U.S. Patent No. 6,205,564 to Kim *et al.* (the "Kim patent").

As previously mentioned, claims 4, 5, 11, 12, 18, 19, 26, 27, 31, and 32 have been cancelled. Consequently, the Examiner's rejection of these claims is now moot.

With respect to the Examiner rejection of claims 1, 15, and 28 under obviousness-type double patenting, claims 1, 15, and 28 have been amended. As amended, these claims no

longer conflict with claims 1, 3, and 7 of the Jeddeloh I patent. Therefore, the Examiner's rejection of these claim under obviousness-type double patenting should now be withdrawn.

With respect to the Examiner's rejection of claims 9-14 under 35 U.S.C. 112, second paragraph, the Examiner objects to the phrase, "a link interface and memory device interface controller" recited in claim 9. The Examiner has interpreted this phrase as reciting "a link interface" and a separate "a memory device interface controller," which then conflicts with the recitation of "a link interface" at line 3 of claim 9. The intended meaning of the phrase "a link interface and memory device interface controller" at line 18 of claim 9 is to recite a "controller" for both the memory device interface as well as for the link interface, and not a controller for just the memory device interface, as interpreted by the Examiner. As a result, the "link interface and memory device interface controller" does not conflict with the "link interface" recited earlier in claim 9. The rejection of claims 9-14 under 35 U.S.C. 112, second paragraph, should be withdrawn.

As previously mentioned, claims 1 and 15 were rejected under 35 U.S.C. 102(b) as being anticipated by the Jeddeloh II patent and claims 1, 15, 23-25, and 28-30 were further rejected under 35 U.S.C. 102(e) as being anticipated by the Wang reference. Claims 1, 15, 23, and 28 have been amended to include limitations that are not described in either the Jeddeloh II or the Wang reference. Therefore, the Examiner's rejection of claims 1 and 15 under 35 U.S.C. 102(b) and claims 1, 15, 23-25, and 28-30 under 35 U.S.C. 102(e) should be withdrawn.

Claims 1, 15, 23, and 28 have been amended to include limitations similar to dependent claims 4 and 5, 11 and 12, 18 and 19, 27, and 32, respectively. The limitations of the dependent claims were rejected by the Examiner under 35 U.S.C. 103(a) as being unpatentable over the Wang reference in view of the Maekawa patent and as being unpatentable over the Wang reference in view of the Hassoun reference. *See* the Office Action at pages 23-25 and 30-31.

The Maekawa patent has been cited by the Examiner as teaching a link interface that includes transmitter and receiver logic having adjustable timing and voltage levels, the timing and voltage levels adjusted according to control signals generated by the memory hub diagnostic engine. *See* the Office Action at page 23. The Maekawa patent is directed to a test system for a semiconductor device that include first, second and third testing units 100, 200, 300

for generating a pattern of input signals for the semiconductor device, and comparing output signals from the semiconductor device to expected data. Each of the testing units receives a different input pattern signal Xin, Yin, Zin, and a different expected pattern signal Xexp, Yexp, Zexp. Operation of the first, second, and third testing units 100, 200, 300 are coordinated to test the semiconductor device against the different test patterns. The first, second, and third testing units 100, 200, 300 are described as having timing generators to coordinate operation of the testing units and adjust the timing at which the input patterns are applied to and the expected data are received from the semiconductor device. The testing units 100, 200, 300 of the Maekawa reference are not analogous to the link interfaces recited in claims. For example, the testing units 100, 200, 300 do not have adjustable voltage levels that are adjusted according to link interface control signals. Each testing unit includes a respective voltage generator 101, 201, 301. As described in the Maekawa reference, the voltage generators 101, 201, 301 are used to generate the input pattern signal for testing the semiconductor device and do not provide for adjusting a voltage of the input signal, for example, adjusting the voltage of a HIGH logic level output. As shown in Figure 4, and described at col. 3, lines 40-60, the voltage generator 101 is clocked by the timing generator 104, but there is no provision for adjusting the voltage level of the signal generated by the voltage generator 101.

Moreover, neither the Wang reference nor the Maekawa reference describe link interface control signals that are generated by a diagnostic engine to adjust the voltage of the link interfaces. As described in the Maekawa reference, the Xin, Yin, and Zin signals are input pattern signals, the Xexp, Yexp, and Zexp signals are expected data signals for comparison to the output signals of the semiconductor device, and the A1-A3, B1-B3, and C1-C3 signals are timer control signals. In the Wang reference, the diagnostic testing commands, as characterized by the Examiner, include signals Bist_mode 113, TCK 116, Bist_status_en 117, none of which are described as being analogous to diagnostic testing commands that would generate link interface control signals. More specifically, the Bist_mode signal 113 is the signal to start the BIST operation, TCK signal 116 is used as the clock to drive the scan chain and the boundary-scan chain, and Bist_status_en 117 is used as an enable signal to shift the memory selector and BIST status chain. As described in the Wang reference, none of these signals provide control of or adjustment of timing or voltage of memory command signals.

The Hassoun patent has been cited by the Examiner as teaching a memory device interface including output buffers having adjustable slew rate and drive strength that are adjusted according to memory device interface control signals. *See* the Office Action at page 25. The Hassoun patent describes a synchronous DRAM ("SDRAM") controller that can be implemented using a programmable logic device ("PLD"). The controller is not described as performing any testing on the SDRAMs being controlled, nor generating diagnostic testing commands. The PLD SDRAM controller described in the Hassoun patent forms a controller and interface between a system and a SDRAM so that functions of the controller can be controlled and changed by simply reprogramming the PLD. The material in the Hassoun patent cited by the Examiner (col. 14, lines 40-42) describes control of the output buffer 1005 of an I/O block 1000, for example, controlling the tristate (i.e., high-z) condition of the output buffer 1005 by use of the tristate signal T and the output of the flip-flop 1001, which maintains the tristate condition of the output buffer 1005 even after the tristate signal T is deasserted. The Hassoun patent further describes the use of an external voltage supply to set the output HIGH voltage of the I/O block 1000, which can then be used to provide the drive capability of the output buffer 1005. The drive strength and slew rate of the output buffer 1005 can then be controlled by using standard methods to configure the external voltage supply appropriately. The drive strength and slew rate, however, are not described as being adjustable, and moreover, are not described as being adjustable using memory device interface control signals generated in response to corresponding diagnostic testing commands.

The Examiner further cited the Hassoun patent as teaching monitoring link interfaces, citing the material at col. 15, lines 2-3. *See* the Office action at pages 30-31. The material cited by the Examiner describes the use of pull-up and pull-down resistors 1008/1009 and a weak keeper circuit 1007 to maintain the logic level of the last output signal, even after the output buffer 1005 returns to a tristate condition. Maintaining the last output state, however, is not the same as monitoring the link interfaces or adjusting at least one of slew rate and drive strength of the link interfaces. Typically, upon returning to a tristate condition the output of the output buffer 1005 will be indeterminate. However, by using the pull-up and pull-down resistors 1008/1009 and the weak keeper circuit 1007, the output of the buffer 1005 is held to the last output state.

The Examiner argues that it would have been obvious to combine the teachings of the Maekawa reference and the Hassoun patent with the teachings of the Wang reference. Assuming for the sake of argument that this is true, the combined teachings of the Wang reference and either the Maekawa reference or the Hassoun patent do not teach or suggest the combination of limitations recited by amended claims 1, 9, 15, 23, and 28. Therefore, the rejection of claims 1, 9, 15, 23, and 28 under 35 U.S.C. 103(a) as being unpatentable over the Wang reference in view of either the Maekawa reference or the Hassoun patent should be withdrawn.

Claims 2, 3, and 6-8, which depend from claim 1, claims 10, 13, and 14, which depend from claim 9, claims 16, 17, 20-22, which depend from claim 15, claims 24 and 25, which depend from claim 23, and claims 29 and 30, which depend from claim 28, are similarly patentable based on their dependency from respective allowable base claims. As previously mentioned, the Examiner has cited the Kanapathippillai patent, Cheung reference, Ku reference, and Kim patent as teaching various limitations of the dependent claims. Even if we assume that the Examiner's characterization of the cited references is accurate, none of them make up for the deficiencies of the Maekawa reference and the Hassoun patent, as previously discussed. Therefore, the Examiner's rejection of claims 2, 3, 6-10, 13, 14, 16, 17, 20-22, 24, 25, 29, and 30 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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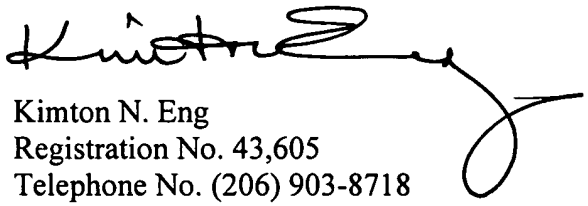

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